

Appln No.: 10/051,990 Applicant(s): Philip Brown et al.

CONFIGURABLE VIRTUAL OUTPUT QUEUES IN A

SCALABLE SWITCHING SYSTEM

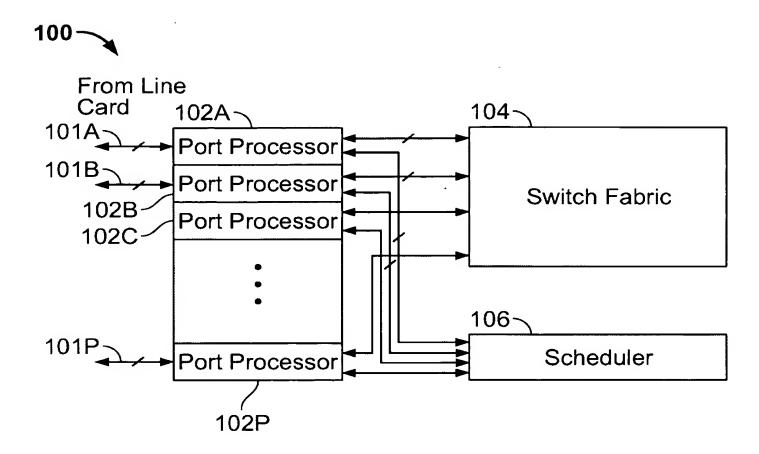


FIG. 1

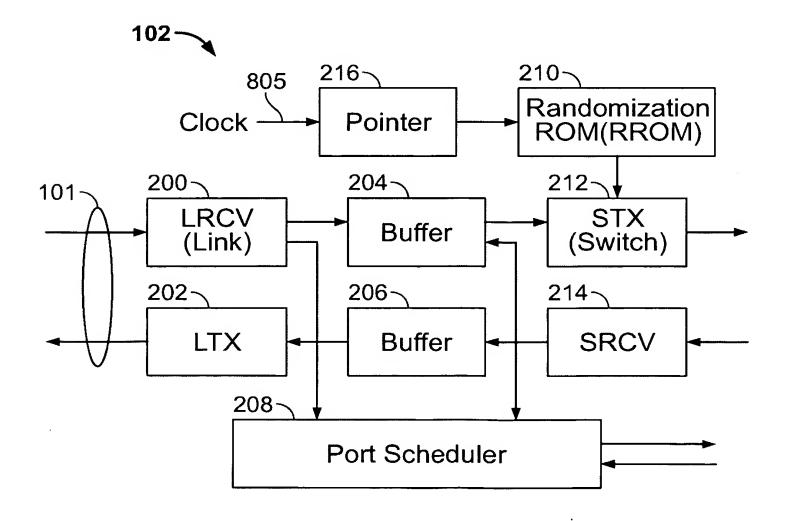


FIG. 2



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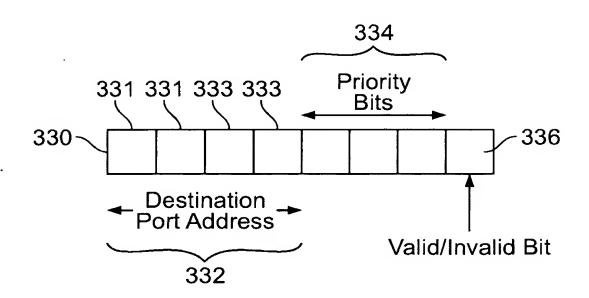


FIG. 3A

204~	\		•				
							300
		,	8	0	4	0 -	310 302
<u>;</u> ;					5	1 -	312 304
				6	2	2	314 306
		15	11	3	3	7 -	316 308
	Queue Splitting:						

FIG. 3B

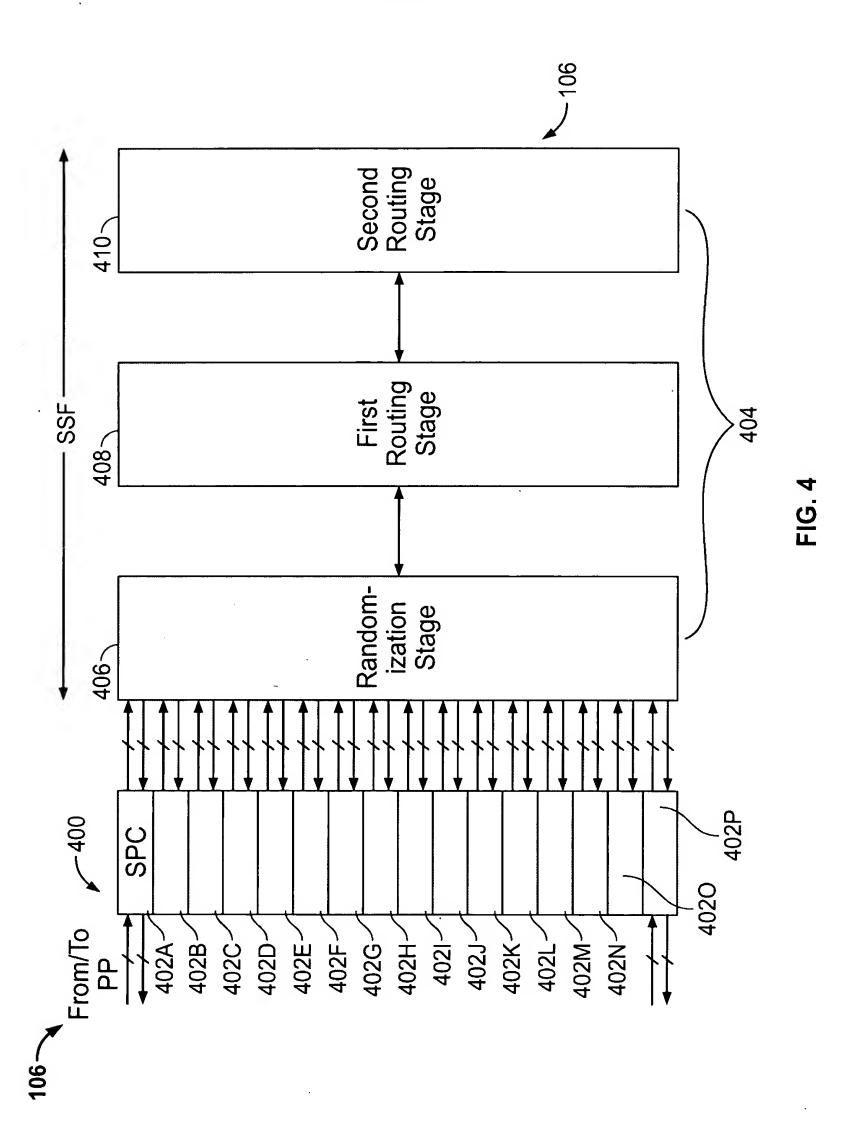


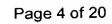
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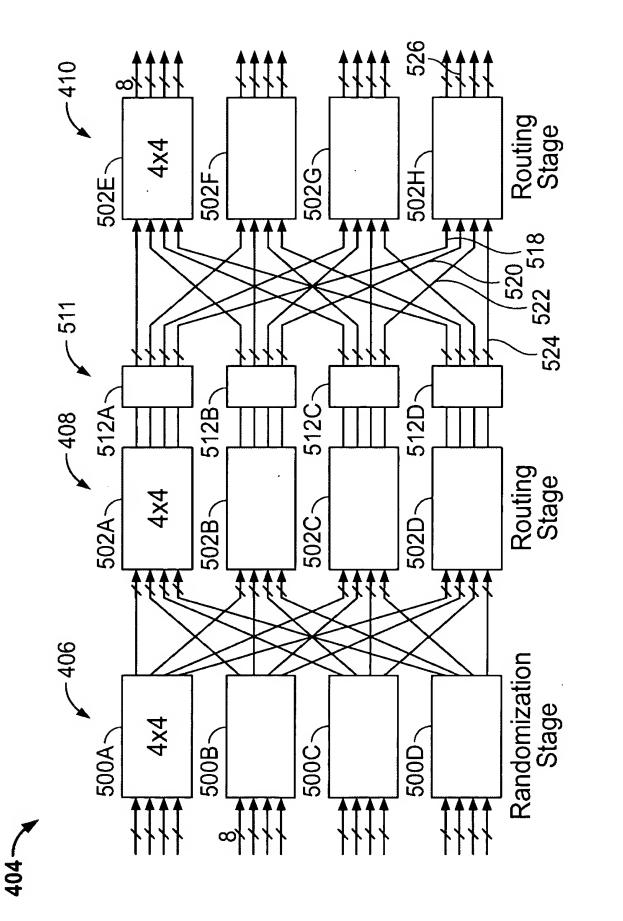






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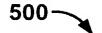




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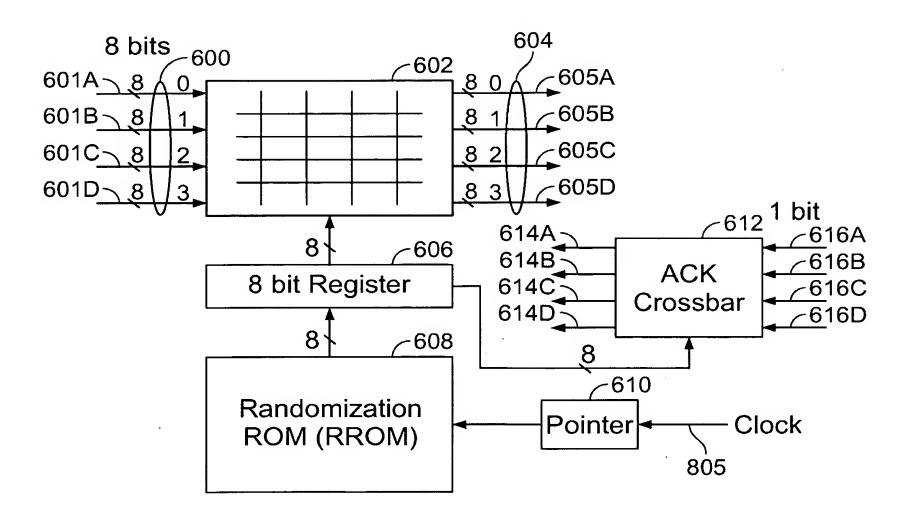
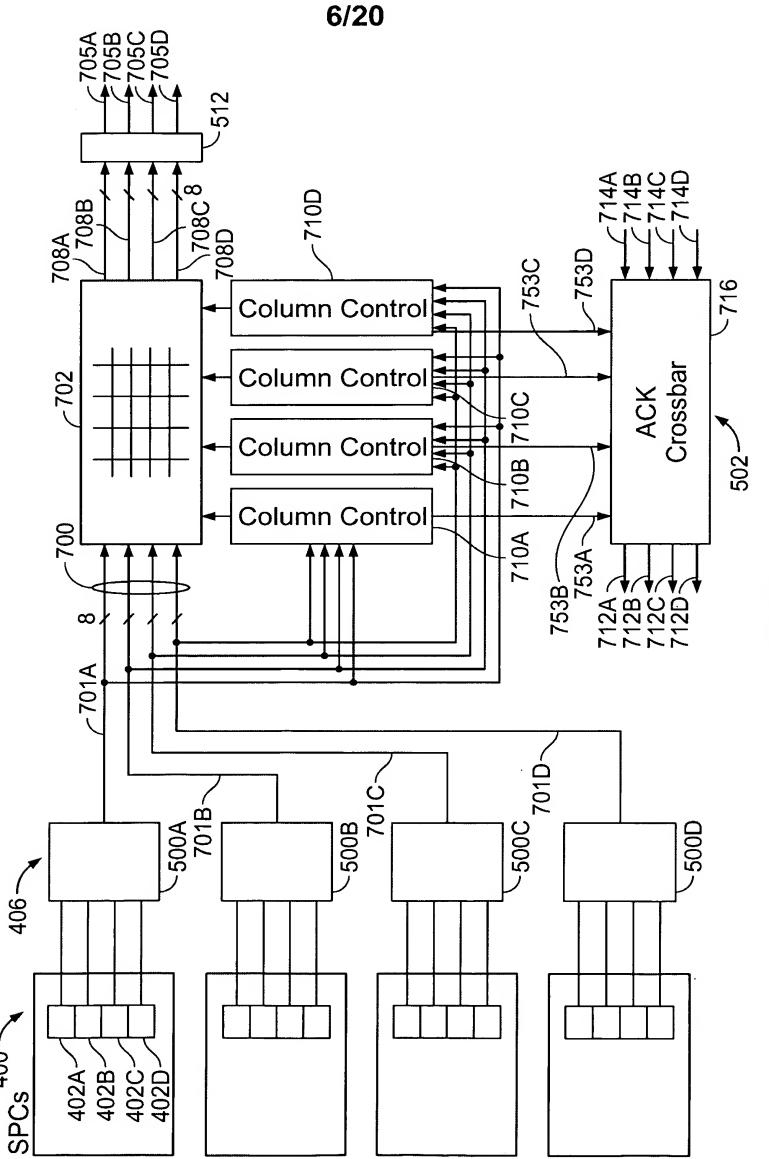


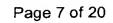
FIG. 6

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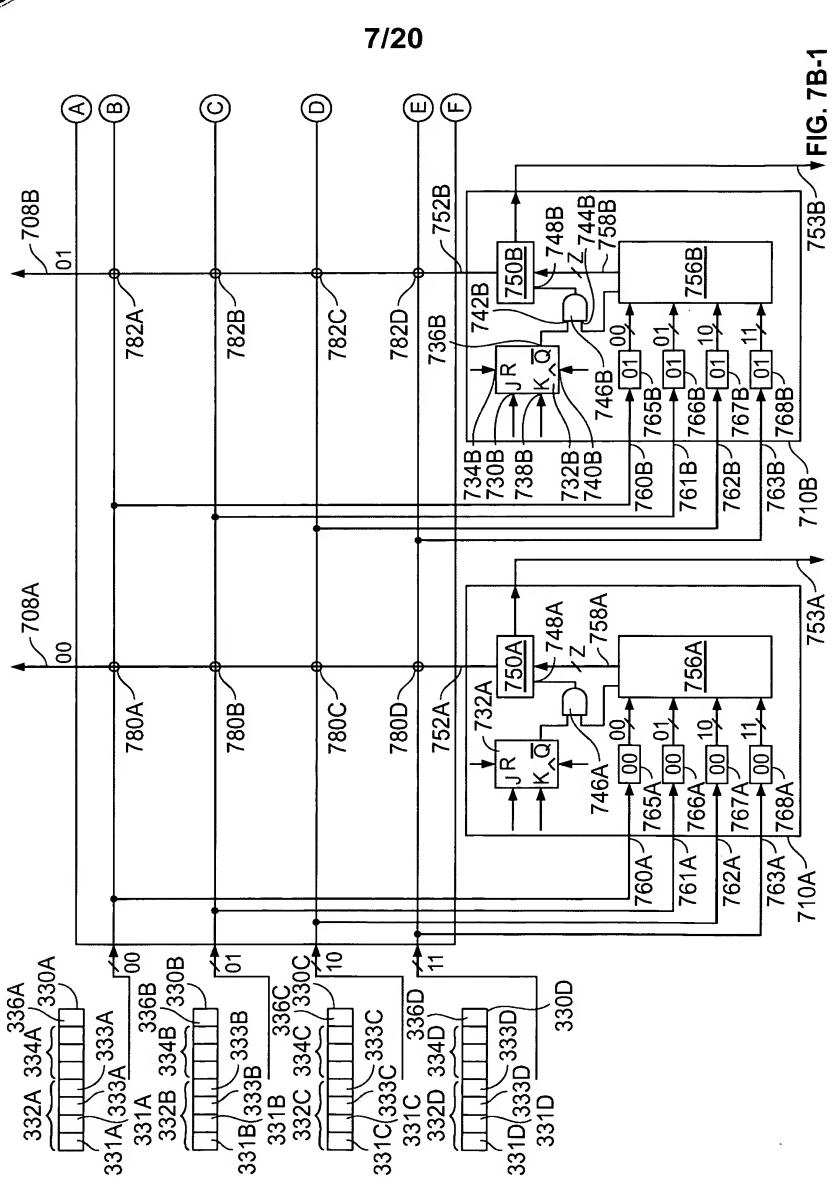






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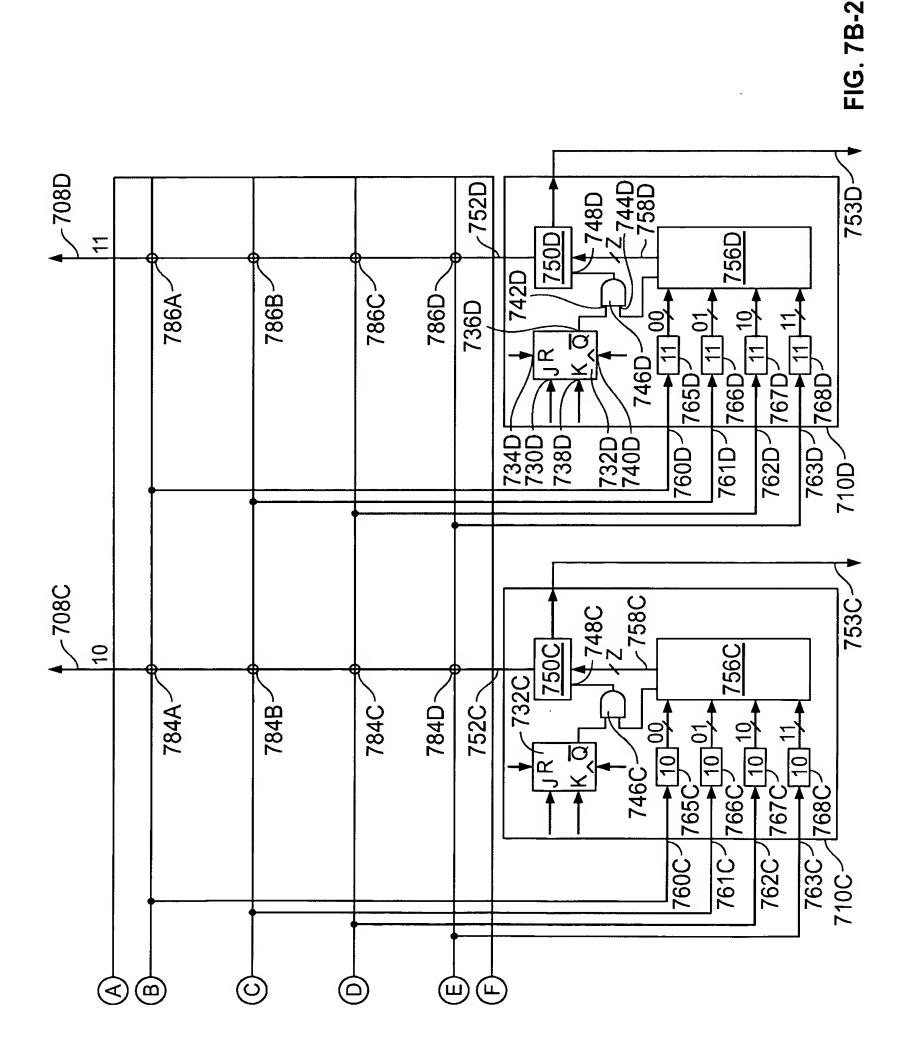




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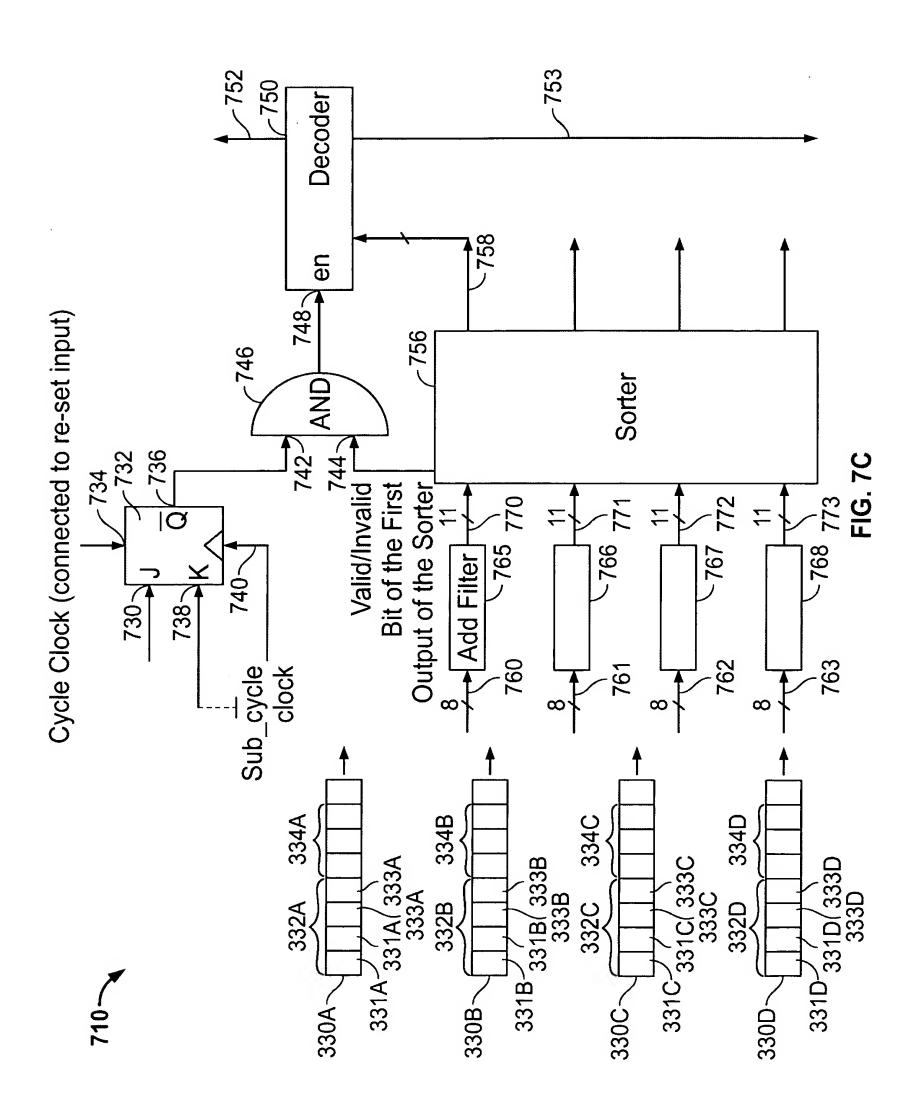
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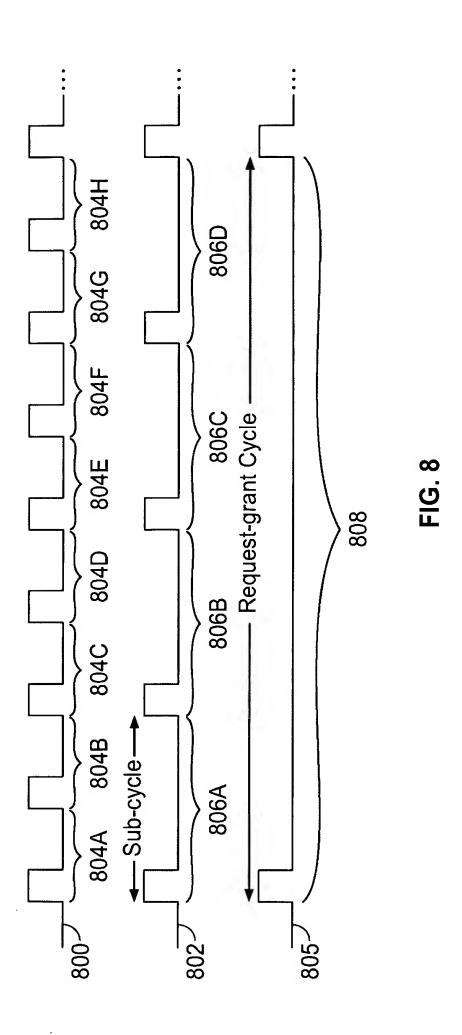




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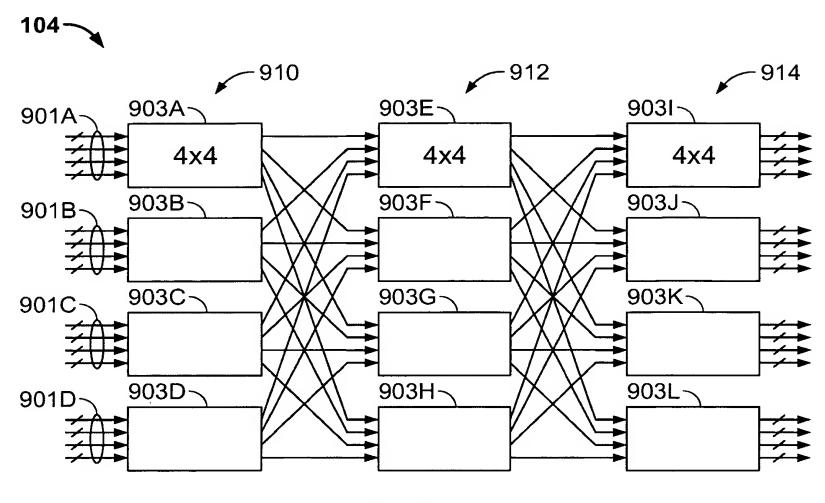


FIG. 9A

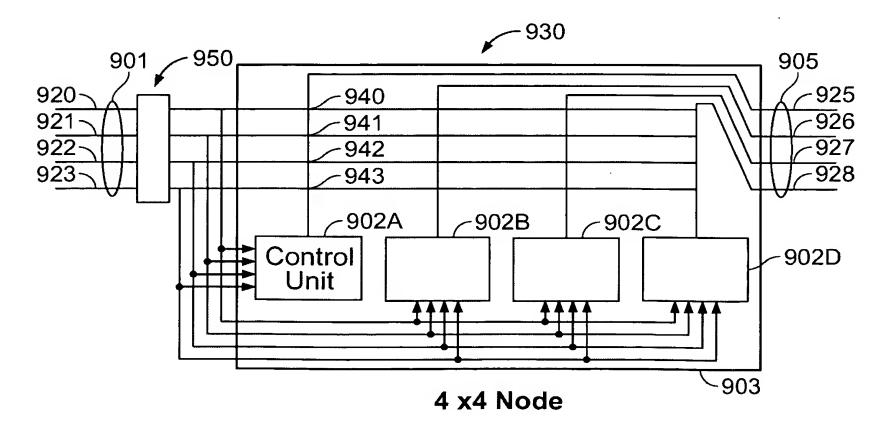


FIG. 9B



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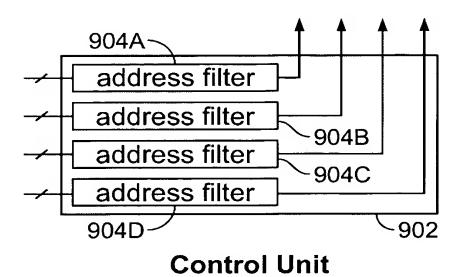


FIG. 9C

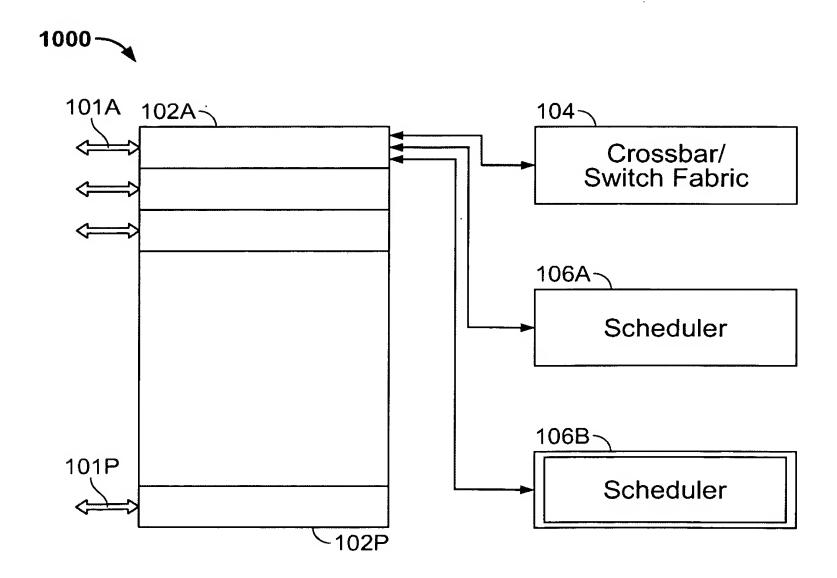


FIG. 10



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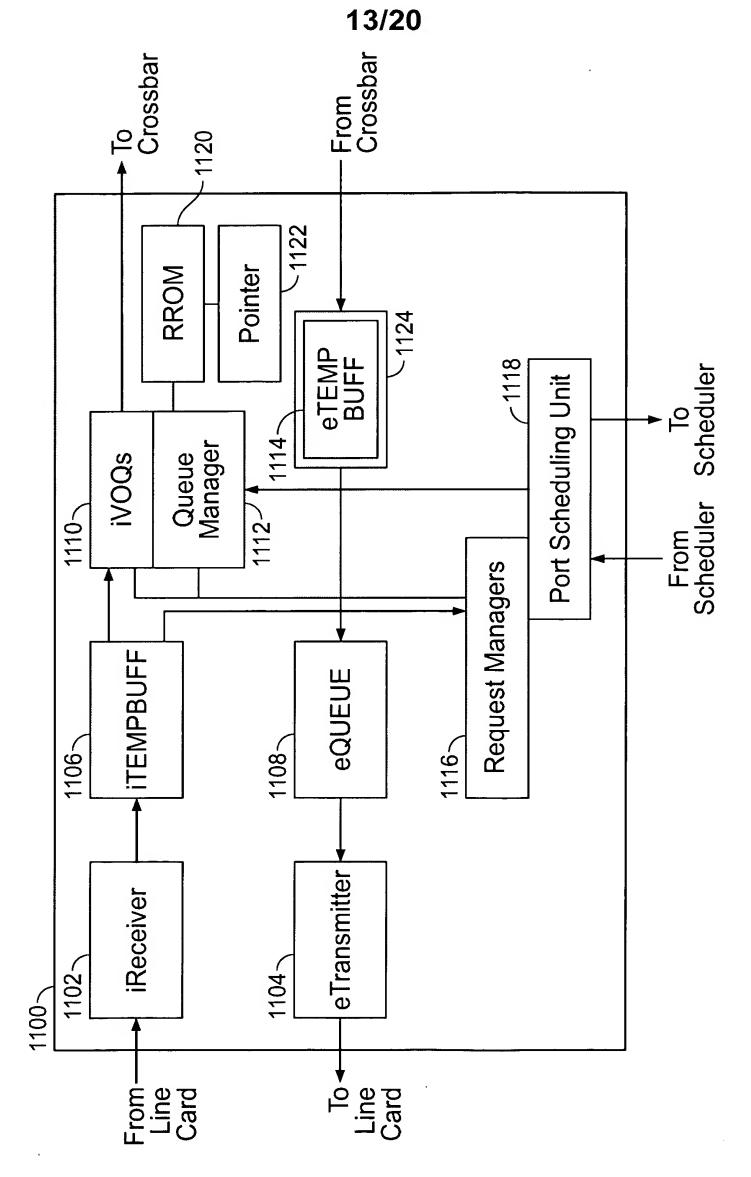


FIG. 11A



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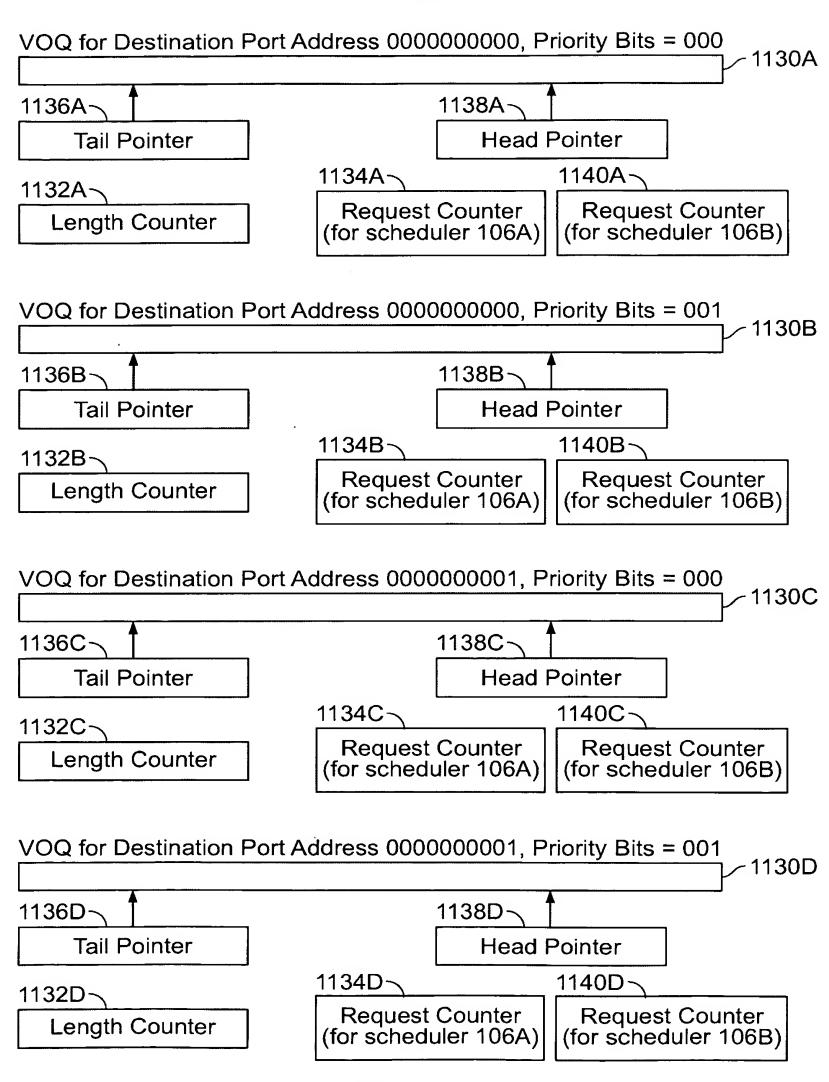
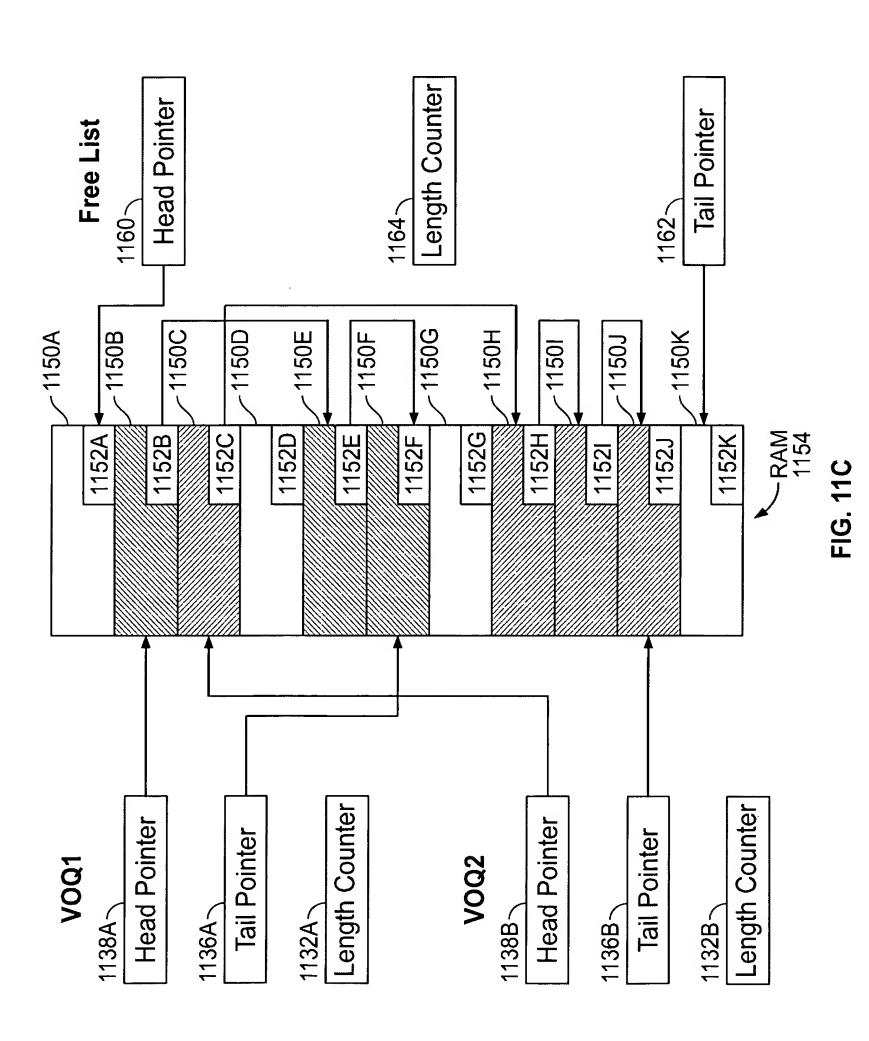


FIG. 11B



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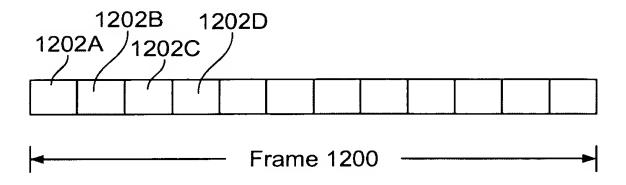


FIG. 12

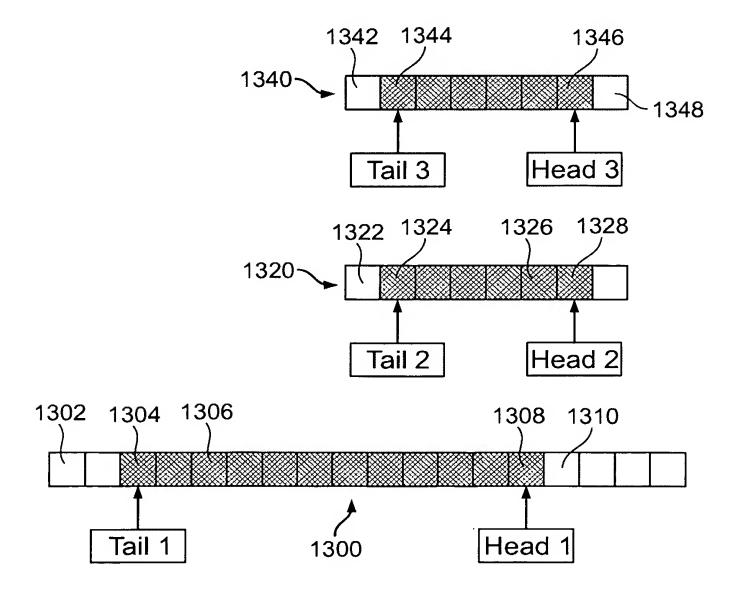


FIG. 13

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1400

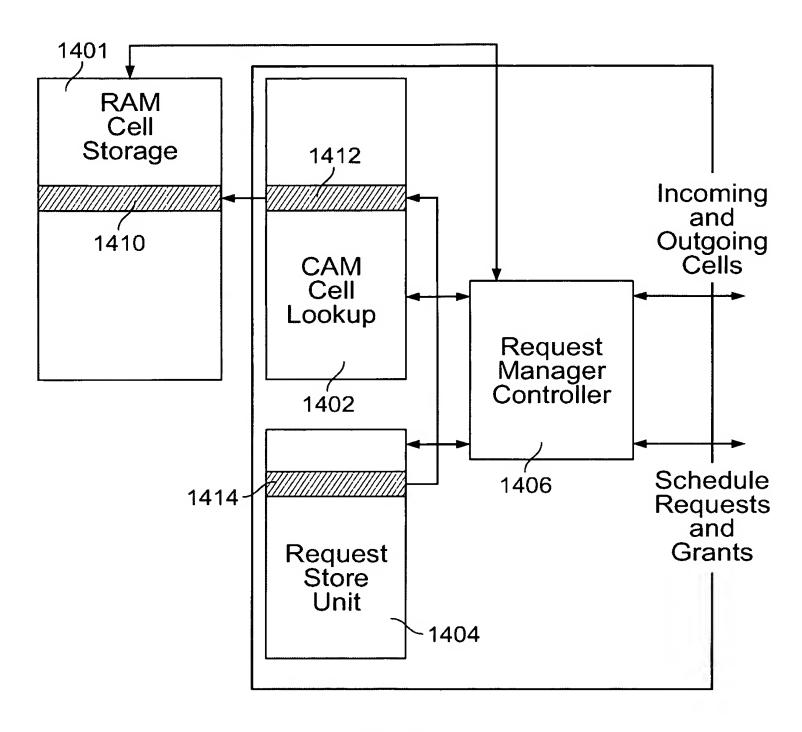


FIG. 14

Cell Lookup CAM Entry Format

Bit[0]	Valid
Bits[10:1]	Pointer
Bits[13:11]	Priority
Bits[24:14]	Destination Address

FIG. 15



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Unicast Request Store Entry Format

Bit[0]	Valid
Bits[7:1]	Priority
Bits[19:8]	Destination Address0
Bits[23:20]	Request Count
Bits[33:24]	Head Pointer
Bits[43:34]	Tail Pointer
Bit[44]	Queue Over Limit
Bit[45]	Flow Control

FIG. 16A

Bit[0]	Valid
Bits[3:1]	Priority
Bits[15:4]	Destination Address0
Bits[19:16]	Request Count
Bits[29:20]	Head Pointer
Bits[39:30]	Tail Pointer
Bit[40]	Flow Control

FIG. 16B



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19/20 Multicast Request Store Entry Format

Bit[0]	Valid
Bits[3:1]	Priority
Bits[7:4]	Cell Requested
Bits[11:8]	Cell Sent
Bits[15:12]	Flow Control
Bits[25:16]	Cell Address
Bits[37: 26]	Destination Address0
Bits[49: 38]	Destination Address1
Bits[61: 50]	Destination Address2
Bits[73: 62]	Destination Address3

FIG. 17

1800~

Receive Unicast Cell; Examine Destination Address and Priority Level of Received Cell

1802~

Locate or Create an Entry in the Unicast Request Store Unit that has the Same Destination Address and Priority Level as the Received Cell

1804-

Locate an Available entry in the CAM; Transfer the Destination Address, Priority Level and Tail Pointer from the Request Store Entry to the Destination Address, Priority Level and Pointer Fields of the Located Entry in the CAM and Assert the Valid Bit of the CAM Entry

1806-

Write the Received Cell into a Memory Location in the RAM that Corresponds to the Address of the new CAM Entry

1808-

Increment the Tail Pointer of the Entry in the Request Store Unit



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1900-

Receive a Request Grant from the Scheduler; Find an Entry in the Request Store Unit with a Destination Address and Priority Level that Match the Destination Address and Priority Level of the Request Grant

1902-

Send the Destination Address, Priority Level and Head Pointer of the Found Entry in the Request Store Unit to the CAM or Control Logic Coupled to the CAM; Find an Entry in the CAM with a Destination Address, Priority Level and Pointer Value that Match the Destination Address, Priority Level and Head Pointer Value of the Found Entry in the Request Store Unit

1904-

Output an Address of the CAM Entry with a Destination Address, Priority Level and Pointer Value that Match the Destination Address, Priority Level and Head Pointer Value of the Entry in the Request Store Unit; Use the Address of the CAM Entry to Retrieve a Cell Stored in a Memory Location of the RAM with the Same Address

1906-

Send the Retrieved Cell to the Switch Fabric for Switching; Increment the Head Pointer of the Request Store Unit Entry; If the VOQ is now Empty, Invalidate the Request Store Unit Entry; If the VOQ is not Empty, Decrement the Request Count Field in the Request Store Unit Entry; Invalidate CAM Entry